

FILE 'USPATFULL' ENTERED AT 09:40:35 ON 30 JAN 2001

09/281,973

L1 40951 S LOGIC CIRCUIT  
L2 28464 S RESET SIGNAL#  
L3 67305 S CLOCK SIGNAL#  
L4 2029779 S FIRST OR PRIMARY SIGNAL#  
L5 43974 S SECOND SIGNAL# OR SECONDARY SIGNAL#  
L6 36982 S L4 (P) (L2 OR L3)  
L7 1848 S L5 (P) (L2 OR L3)  
L8 7484 S L1 AND L6  
L9 365 S L8 AND L7  
L10 1583 S L6 (P) L7  
L11 59 S L1 (P) L10  
L12 5312 S TEST CIRCUIT OR TEST MODE RELATED CIRCUIT  
L13 1 S L11 (P) L12  
SAVE TESTCIRCUIT/L ALL  
L14 307702 S COUNTER#  
L15 8539 S COUNT### (W) SIGNAL#  
L16 6371 S L14 (P) L15  
L17 1 S L16 (P) L11  
L18 1 S L12 (P) L11  
SAVE TESTCIRCUIT/L ALL

=> d l17 ibib ti

L17 ANSWER 1 OF 1 USPATFULL

ACCESSION NUMBER: 95:12224 USPATFULL

TITLE: Parallel computer system including request  
distribution

INVENTOR(S): network for distributing processing requests to  
selected sets of processors in parallel  
Leiserson, Charles E., Winchester, MA, United States  
Zak, Jr., Robert C., Lexington, MA, United States  
Hillis, W. Daniel, Cambridge, MA, United States  
Kuszmaul, Bradley C., Waltham, MA, United States  
Hill, Jeffrey V., Santa Clara, CA, United States  
PATENT ASSIGNEE(S): Thinking Machines Corporation, Cambridge, MA, United  
States (U.S. corporation)

|                       | NUMBER  | DATE         |
|-----------------------|---|--------------|
| PATENT INFORMATION:   | US 5388214  | 19950207     |
| APPLICATION INFO.:    | US 1994-183219  | 19940114 (8) |
| RELATED APPLN. INFO.: | Division of Ser. No. US 1992-946242, filed on 16 Sep<br>1992, now patented, Pat. No. US 5333268 which is a<br>continuation of Ser. No. US 1990-592029, filed on 3 |              |

Oct

1990, now abandoned

DOCUMENT TYPE: Utility

PRIMARY EXAMINER: Richardson, Robert L.

LEGAL REPRESENTATIVE: Jordan, Richard A.

NUMBER OF CLAIMS: 31

EXEMPLARY CLAIM: 1

NUMBER OF DRAWINGS: 84 Drawing Figure(s); 79 Drawing Page(s)

LINE COUNT: 12480

TI Parallel computer system including request distribution network for  
distributing processing requests to selected sets of processors in  
parallel

=> d 118 ibib ti

L18 ANSWER 1 OF 1 USPATFULL

ACCESSION NUMBER: 1998:59117 USPATFULL  
TITLE: SDRAM clocking test mode  
INVENTOR(S): Manning, Troy A., Boise, ID, United States  
PATENT ASSIGNEE(S): Micron Technology, Inc., Boise, ID, United States  
(U.S. corporation)

|                       | NUMBER                                 | DATE         |
|-----------------------|--|--------------|
| PATENT INFORMATION:   | US 5757705                             | 19980526     |
| APPLICATION INFO.:    | US 1997-787149                         | 19970122 (8) |
| DOCUMENT TYPE:        | Utility                                |              |
| PRIMARY EXAMINER:     | Yoo, Do Hyun                           |              |
| LEGAL REPRESENTATIVE: | Seed and Berry LLP                     |              |
| NUMBER OF CLAIMS:     | 39                                     |              |
| EXEMPLARY CLAIM:      | 1                                      |              |
| NUMBER OF DRAWINGS:   | 6 Drawing Figure(s); 5 Drawing Page(s) |              |
| LINE COUNT:           | 698                                    |              |
| TI                    | SDRAM clocking test mode               |              |

=> d 118 kwic

L18 ANSWER 1 OF 1 USPATFULL

CLM What is claimed is:

5. A **test circuit** for providing a **test clock signal** to a SDRAM of the type having an internal clock input, the **test circuit** and the SDRAM being housed in a common package having a clock terminal adapted to receive a **clock signal**, a clock enable terminal adapted to receive a clock enable signal and at least one additional terminal adapted to receive an additional signal, the **test circuit** comprising a **logic circuit** having inputs coupled to the clock terminal, the clock enable terminal, and the additional terminal of the package, and an output coupled to the internal clock input of the SDRAM, the **logic circuit** coupling the clock terminal to the output of the **logic circuit** responsive to the clock enable signal being active and the additional terminal receiving a **first signal**, the **logic circuit** deriving the **test clock signal** from respective periodic signals applied to the clock and clock enable terminals and applying the **test clock signal** to the output of the **logic circuit** when the additional terminal receives a **second signal**, the **test clock signal** having a frequency that is greater than the frequencies of either of the periodic signals.

=> d 117 ab

L17 ANSWER 1 OF 1 USPATFULL

AB A computer comprising a plurality of processing nodes, a control node and a request distribution network. Each processing node receives processing requests and generates in response processed data. The control node generates processing requests for transfer to selected ones

of the processing nodes as identified by associated request address information, receives processed data in response, the request address information identifying selected ones of the processing nodes to receive a processing request in parallel. The request distribution network distributes the processing requests to the processing nodes and returns processed data to the control node. The network includes a plurality of request distribution nodes connected in a plurality of levels to form a tree-structure, including an upper root level and a lower leaf level. Each request distribution node is connected to receive processing requests from, and to couple processed data to, a parent, the parent of the request distribution node of the root level comprising the control node, and each request distribution node being further connected to couple processing requests to and receive processed data from, selected children, the children of the request distribution nodes of the leaf level comprising the processing nodes. Each request distribution node, in response to request address information received from its parent, identifies selected ones of its children and thereafter couples further request address information which it receives and processing requests in parallel to its children.